Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Please amend the claims as follows:

1-18. (Cancelled).

19. (Previously Presented) A device comprising:

first circuitry to generate a packet based on packet header data received from and generated by a micro-engine and packet payload data from a memory controller, wherein the packet payload data bypasses the micro-engine, the first circuitry comprising

second circuitry to receive the packet payload data from the memory controller, and to store the packet payload data in first-in first-out (FIFO) circuitry; and

third circuitry to track a start lane in the FIFO circuitry indicating a start of free space in the FIFO circuitry, and to determine a starting lane for the packet payload data such that alignment of the packet payload data matches the start lane in the FIFO circuitry.

20. (Previously Presented) The device of claim 19, wherein the second circuitry comprises:

logic to synchronize receipt of the packet header data from the micro-engine and the packet payload data from the memory controller, to store the packet header data in the FIFO circuitry, and

to transfer the packet header data and packet payload data from the FIFO circuitry to a destination specified in the packet header.

21. (Previously Presented) The device of claim 19, wherein the micro engine is a direct memory access (DMA) controller send queue to transmit requests and receive responses.

22. (Previously Presented) The device of claim 19, wherein the micro engine is a direct memory access (DMA) controller receive queue to transmit response and receive requests.

23. (Previously Presented) A method comprising:

receiving packet header data generated by a micro-engine;

storing the packet header data in the FIFO queue;

receiving packet payload data from a memory controller, wherein the packet payload data bypasses the micro-engine; and

storing the packet payload data in a first-in first-out (FIFO) queue, wherein the storing includes

tracking a start lane in the FIFO queue indicating a start of free space in the FIFO queue,

determining a starting lane for the packet payload data such that alignment of packet payload data matches the start lane in the FIFO queue.